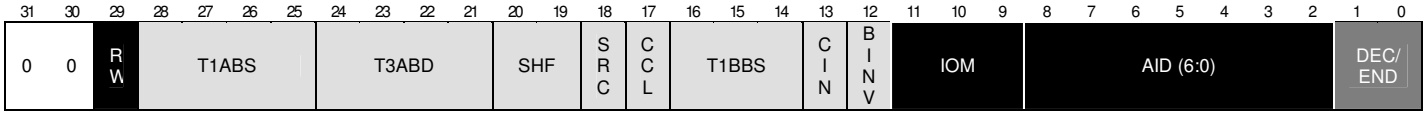
TPU REFERENCE MANUAL TPURM/AD

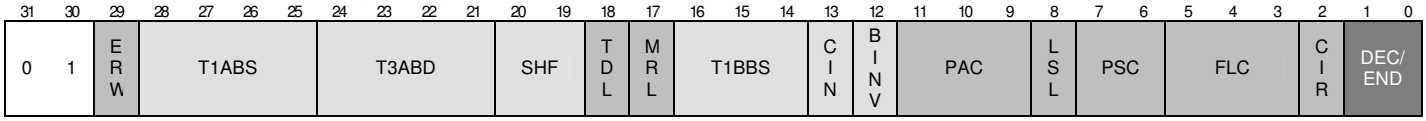
APPENDIX B
MICROINSTRUCTION FORMATS AND ENCODINGS

The following formats are named according to the major activities performed by the microinstruction and, in the illustration, are shaded according to the applicable operations:

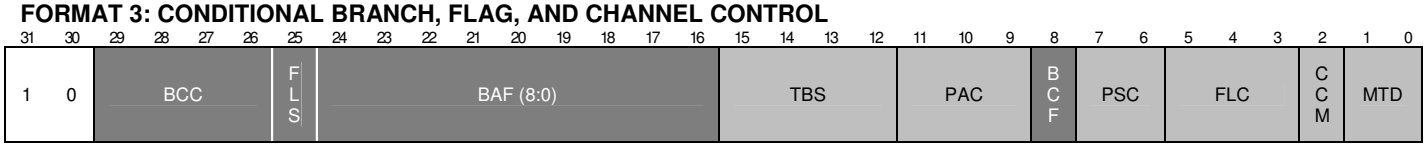
FORMAT 1: EXECUTION UNIT AND RAM



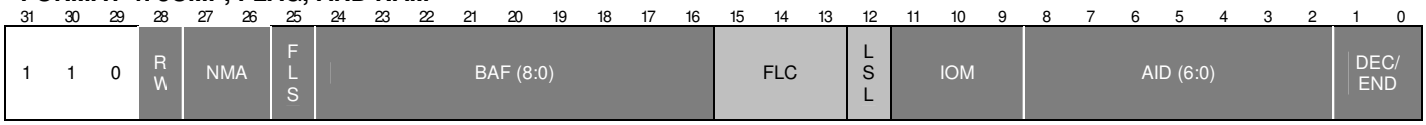
FORMAT 2: EXECUTION UNIT, FLAG, AND CHANNEL CONTROL



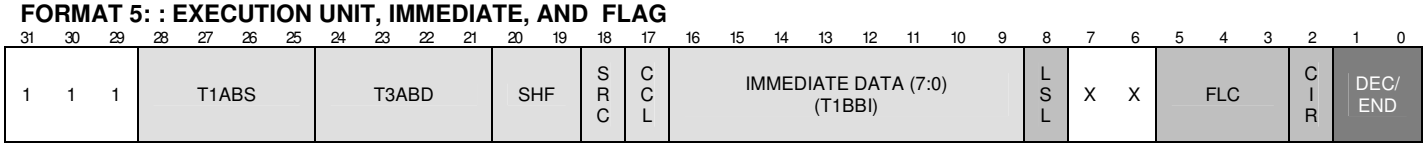
FORMAT 3: CONDITIONAL BRANCH, FLAG, AND CHANNEL CONTROL



FORMAT 4: JUMP, FLAG, AND RAM



FORMAT 5: : EXECUTION UNIT, IMMEDIATE, AND FLAG



EXECUTION UNIT OPERATIONS

MICROENGINE/SEQUENCING OPERATIONS

CHANNEL CONTROL OPERATIONS

RAM INPUT/OUTPUT OPERATIONS

The following text provides the microinstruction encodings and timings. Although each format is subdivided by the operations applicable to that format, the fields maintain their order of appearance per the illustration, from most significant bit to least significant bit. Consequently, this order references some fields in an unrelated operation. For remedy, cross referencing is used to identify the correct operation. Below is a list of acronyms used in addition to the acronyms identified within the encodings and timings:

=	Indicates Bit Value Equivalence
A	Accumulator Register (General- Purpose)
AB	A-Bus
AU	Arithmetic Unit
BB	B-Bus
CHAN	Channel Number Register
DEC	Decrementor
DIOB	Data Input/Output Buffer Register
ERT	Event Register Temporary
LINK	Encoded Link Register
MER	Match Event Register
P	Parameter Register
RAR	Return Address Register
SR	Shift Register (Execution Unit)
µPC	Microprogram Counter

B.1 Format 1: Execution Unit and RAM

B.1.1 Execution Unit Operations

R/W - See B.1.2 RAM Operations

T1 ABS - T1 A-Bus Source Control

BYTE Source

0000	AB(7:0)	= P(7:0);	AB(8:15)	=0	(t1)
0001	AB(7:0)	= P(15:8);	AB(8:15)	=0	(t1)
0010	AB(3:0)	= DEC(3:0);	AB(4:15)	=0	(t1)
0011	AB(7:4)	= CHAN(3:0);	AB(0:3), AB(8:15)	=0	(t1)
0111	AB(7:0)	=00;	AB(8:15)	=0	(t1)

SPECIAL OPERATION (byte operation with respect to AU flags)

0100	AB(15:0)=0;	ERT	= MER	(t2)

WORD Source

1000	AB(15:0)	= P(15:0)	(t1)
1001	AB(15:0)	= A(15:0)	(t1)
1010	AB(15:0)	= SR(15:0)	(t1)
1011	AB(15:0)	= DIOB(15:0)	(t1)
1100	AB(15:0)	= TCR1 (15:0)	(t1)
1101	AB(15:0)	= TCR2(15:0)	(t1)
1110	AB(15:0)	= ERT(15:0)	(t1)
1111	AB(15:0)	= 0000	(t1)

T3ABD - T3 A-Bus Destination Control

0000	A(15:0)	= AB(15:0)	(t3)
0001	SR(15:0)	= AB(15:0)	(t3)
0010	ERT(15:0)	= AB(15:0)	(t3)
0011	DIOB(15:0)	= AB(15:0)	(t3)
0100	P(15:8)	= AB(7:0)	(t3)
0110	P(7:0)	= AB(7:0)	(t3)
0111	P(15:0)	= AB(15:0)	(t3)
1000	LINK(3:0)	= AB(7:4)	(t3)
1001	CHAN(3:0)	= AB(7:4)	(t3)
1010	DEC(3:0)	= AB(3:0)	(t3)
1011	DEC(3:0)	= AB(3:0); CHAN(3:0) = AB(7:4)	(t3)
1100	TCR1 (15:0)	= AB(15:0)	(t3)
1101	TCR2(15:0)	= AB(15:0)	(t3)
1111	Nil (No destination is selected)		

SHF - AU Shifter Control

00 (Shift left)
AB(15:1) = AU(14:0), AB(0) = 0 (t3)
Carry latch = AU(15)

01 (Shift right)
if SRC = 1 then
AB(14:0) = AU(15:1), AB(15) = Cout of AU (t3)
else
AB(14:0) = AU(15:1), AB(15) = 0 (t3)
Carry latch = AU(0)

10 (Rotate right)
AB(14:0) = AU(15:1), AB(15) = AU(0) (t3)

Carry latch = AU(0)

11 (No shift)
AB(15:0) = AU(15:0) (t3)
Carry latch = Cout of AU

NOTE

1. Cout represents the carryout of the AU-AU(16).
2. Carry latch represents the latch that is an input into the branch PLA.
3. Encoding CCl controls the latching of the carry latch.
4. When SHF = 11 and a byte operation is performed, Cout is generated from the lower byte of the result. Otherwise, Cout is generated from the word result.

SRC - Shift Register Control

0 Shift right: SR(14:0) = SR(15:1)
If SHF = 01 then SR(15) = AU(0)
else SR(15) = 0;
1 No shift

CCL - AU Condition Latch Control

0 Latch conditions Z, C, N, and V into branch PLA (t3)
1 Do not latch conditions Z, C, N, and V

T1BBS - T1 B-Bus Source Control

000	BB(15:0)	= P(15:0)	(t1)
001	BB(15:0)	= A(15:0)	(t1)
010	BB(15:0)	= SR(15:0)	(t1)
011	BB(15:0)	= DIOB(15:0)	(t1)
111	BB(15:0)	= 00000	(t1)

NOTE

If shift right is specified for the AU shifter (SHF = 01), if the shift register is enabled (SRC = 0), and if the decrementor is decrementing, then the B-bus is driven with the register specified by T1 BBS or $0000, determined by the least significant bit of the shift register. If this bit is one, B-bus equals the register specified by T1 BBS, otherwise B-bus is negated.

CIN - AU B-Bus Carry Control

0	Carry in	= 1	(t1)
1	Carry in	= 0	(t1)

NOTE

A special case is the creation of the constant $8000: if (T1 BBS = 111) and (CIN = 0) and (BINV = 0), then B-bus equals $8000. This is implemented by special logic to negate bit 15 of the bus.

BINV - AU B-Bus Invert Control

0	Bin(15:0)	= BB(15:0) INVERTED	(t1)
1	Bin(15:0)	= BB(15:0)	(t1)

B.1.2 RAM Operations

RW - RAM Read/Write Control

0 Parameter access is a read (from RAM)
1 Parameter access is a write (to RAM)

IOM - RAM Input/Output Mode Control

000 P access using three-bit parameter number from AID (2:0) concatenated with channel number from channel register

001 P access using seven-bit address from DIOB (7:1)

010 P access using seven-bit address from AID (6:0)

100 DIOB access using three-bit parameter number from AID (2:0) concatenated with channel number from channel register

101 DIOB access using seven-bit address from DIOB (7:1)

110 DIOB access using seven-bit address from AID (6:0)
x11 Nil

AID - RAM Address

	(7 bits)
xxxxxxx	$00-$7F

B.1.3 Microengine/Sequencing Operations

DEC/END - Decrementor/End State Control

00 Start decrement
When DEC becomes one, the µPC is loaded from the return address register.

01 Start decrement
µPC is not incremented while the decrementor is decrementing, until DEC becomes one.

10 End current state

11 Nil

B.2 FORMAT 2: EXECUTION UNIT, FLAG, AND CHANNEL CONTROL

B.2.1 Execution Unit Operations

ERW - See B.2.2 Channel Control Operations T1 ABS - T1 A-Bus Source Control

BYTE Source

0000	AB(7:0)	= P(7:0);	AB(8:15)	=0	(t1)
0001	AB(7:0)	= P(15:8);	AB(8:15)	=0	(t1)
0010	AB(3:0)	= DEC(3:0);	AB(4:15)	=0	(t1)
0011	AB(7:4)	= CHAN(3:0);	AB(0:3),AB(8:15)	=0	(t1)
0111	AB(7:0)	= 00;	AB(8:15)	=0	(t1)

SPECIAL OPERATION (byte operation with respect to AU flags)

0100	AB(15:0)	=0;	ERT	=MER	(t2)

WORD Source

1000	AB(15:0)	= P(15:0)	(t1)
1001	AB(15:0)	= A(15:0)	(t1)
1010	AB(15:0)	= SR(15:0)	(t1)
1011	AB(15:0)	= DIOB(15:0)	(t1)
1100	AB(15:0)	= TCR1 (15:0)	(t1)
1101	AB(15:0)	= TCR2(15:0)	(t1)
1110	AB(15:0)	= ERT(15:0)	(t1)
1111	AB(15:0)	= 0000	(t1)

T3ABD - T3 A-Bus Destination Control

0000	A(15:0)	= AB(15:0)	(t3)
0001	SR(15:0)	= AB(15:0)	(t3)
0010	ERT(15:0)	= AB(15:0)	(t3)
0011	DIOB(15:0)	= AB(15:0)	(t3)
0100	P(15:8)	= AB(7:0)	(t3)
0110	P(7:0)	= AB(7:0)	(t3)
0111	P(15:0)	= AB(15:0)	(t3)
1000	LINK(3:0)	= AB(7:4)	(t3)
1001	CHAN(3:0)	= AB(7:4)	(t3)
1010	DEC(3:0)	= AB(3:0)	(t3)
1011	DEC(3:0)	= AB(3:0); CHAN(3:0) = AB(7:4)	(t3)
1100	TCR1 (15:0)	= AB(15:0)	(t3)
1101	TCR2 (15:0)	= AB(15:0)	(t3)
1111	Nil	(No destination is selected)	

SHF - AU Shifter Control

00 (Shift left)
AB(15:1) = AU(14:0), AB(0) = 0 (t3)
Carry latch = AU(15)

01 (Shift right)
if SRC = 1 then
AB(14:0) = AU(15:1), AB(15) = Cout of AU (t3)
else
AB(14:0) = AU(15:1),AB(15) = 0 (t3)
Carry latch = AU(O)

10 (Rotate right)
AB(14:0) = AU(15:1), AB(15) = AU(0) (t3)
Carry latch = AU(0)

11 (No shift)
AB(15:0) = AU(15:0) (t3)
Carry latch = Cout of AU

NOTE

1. Cout represents the carryout of the AU-AU(16).
2. Carry latch represents the latch that is an input into the branch PLA.
3. Encoding CCl controls the latching of the carry latch.
4. When SHF = 11 and a byte operation is performed, Cout is generated from the lower byte of the result. Otherwise, Cout is generated from the word result.

TDL - See B.2.2 Channel Control Operations

MRL - See B.2.2 Channel Control Operations

T1 BBS - T1 B-Bus Source Control

000	BB(15:0)	= P(15:0)	(t1)
001	BB(15:0)	= A(15:0)	(t1)
010	BB(15:0)	= SR(15:0)	(t1)
011	BB(15:0)	= DIOB(15:0)	(t1)
111	BB(15:0)	= 00000	(t1)

NOTE

If shift right is specified for the AU shifter (SHF = 01), if the shift register is enabled (SRC = 0), and if the decrementor is decrementing, then the B-bus is driven with the register specified by T1 BBS or $0000, determined by the least significant bit of the shift register. If this bit is one, B-bus equals the register specified by T1 BBS, otherwise B-bus is negated.

CIN - AU B-Bus Carry Control

0	Carry in	= 1	(t1)
1	Carry in	= 0	(t1)

NOTE

A special case is the creation of the constant $8000: if (T1 BBS = 111) and (CIN = 0) and (BINV = 0), then B-bus equals $8000. This is implemented by special logic to negate bit 15 of the bus.

BINV - AU B-Bus Invert Control

0	Bin(15:0)	= BB(15:0) INVERTED	(t1)
1	Bin(15:0)	= BB(15:0)	(t1)

B.2.2 Channel Control Operations

ERW - Event Register Write Control

(One microcycle delay before effect)

0	MER(15:0) = ERT(15:0)	(t2)
1	Nil	

TDL - Transition Detect Latch Negation Control

(One microcycle delay before effect)

0	Negate TDL	(t2)
1	Nil	

MRL - Match Recognition Latch Negation Control

(One microcycle delay before effect)

0	Negate MRL	(t2)
1	Nil	

PAC - Pin Action Control

(One microcycle delay before effect)

	If pin is OUTPUT, on match:	If pin is INPUT, transition detect on:	
000	No change in pin state	No transition	(t2)
001	Set pin high	Low high	(t2)
010	Set pin low	High low	(t2)
011	Set pin to toggle	Any transition	(t2)
1xx	Nil (do not change state of PAC latches)		

LSR - Link Service Request Negation Control

0	Negate LSR
1	Nil

PSC - Pin State Control

(One microcycle delay before effect)

00	Set pin as specified by PAC latches	(t2)
01	Set pin high	(t2)

10	Set pin low	(t2)
11	Nil	

NOTE

If PSC equals 00 and PAC is given value at the same instruction,

FLC - Flag Control

001	Assert flag0	(t2)
000	Clear flag0	(t2)
011	Assert flag1	(t2)
010	Clear flag 1	(t2)
1xx	Nil	

CIR - Channel Interrupt Request

0	Assert channel interrupt bit	(t1)
1	Nil	

B.2.3 Microengine/Sequencing Operations

Decrementor/End State Control (DEC)

00 Start decrement
When DEC becomes one, the µPC is loaded from the return address register.

01 Start decrement
µPC is not incremented while the decrementor is decrementing, until DEC becomes one.

10 End current state

11 Nil

B.3 Format 3: BRANCH, Flag, and Channel Control

B.3.1 Microengine/Sequencing Operations

CJC - Conditional Jump Code Field

0000	Branch on AU LT (= N•$\overline{V}$ + $\overline{N}$•V) = AB source is less than BB source (signed)
0001	Branch on AU LS (= C + Z) = AB source is lower/same as BB source(unsigned)
0010	Branch on AU V bit overflow flag
0011	Branch on AU N bit latch (minus/plus)
0100	Branch on AU C bit latch (high or same/low)
0101	Branch on AU Z bit latch (equal/not equal)
0110	Branch on flag 1
0111	Branch on flag0
1000	Branch on TDL
1001	Branch on MRL
1010	Branch on LSR
1011	Branch on host sequence bit 1
1100	Branch on host sequence bit 0
1101	Branch on pin state latch
1110	Not currently used
1111	Branch condition false

FLS - µPC Flush Control

0	Flush instruction pipe (force microinstruction decode to NOP)
1	Nil

NOTE

If the branch is conditional, then flush is executed if and only if the

jump condition (defined by CJC and BCF) is true.

BAF - Branch Address Field

	(9 bits)
xxxxxxxxx	$000-$1FF

***BCF - Branch Condition False Control**

0	Conditionally branch if specified signal false
1	Conditionally branch if specified signal true

*This field is listed here out of order (BCF occupies bit position 8) for the purpose of identifying it with the correct operation.

B.3.2 Channel Control Operations

TBS - Time Base Select Control

(One microcycle delay before effect)

0000	Input channel;	capture TCR1 ; match TCR1	(match T2; capture T4)
0001	Input channel;	capture TCR1; match TCR2	(match T2; capture T4)
0010	Input channel;	capture TCR2; match TCR1	(match T2; capture T4)
0011	Input channel;	capture TCR2; match TCR2	(match T2; capture T4)
0100	Output channel;	capture TCR1 ; match TCR1	(match T2; capture T4)
0101	Output channel;	capture TCR1; match TCR2	(match T2; capture T4)
0110	Output channel;	capture TCR2; match TCR1	(match T2; capture T4)
0111	Output channel;	capture TCR2; match TCR2	(match T2; capture T4)
1xxx	No change		

PAC - Pin Action Control

(One microcycle delay before effect)

	If pin is OUTPUT, on match:	If pin is INPUT, transition detect on:	
000	No change in pin state	No transition	(t2)
001	Set pin high	Low high	(t2)
010	Set pin low	High low	(t2)
011	Set pin to toggle	Any transition	(t2)
1xx	Nil (do not change state of PAC latches)		

BCF - See B.3.1 MIcroengine/Sequencing Operations Pin State Control (PSC)

(One microcycle delay before effect)

00	Set pin as specified by PAC latches	(t2)
01	Set pin high	(t2)
10	Set pin low	(t2)
11	Nil	

NOTE

If PSC equals 00 and PAC is given value at the same instruction, the pin value will be set by the new PAC value.

FLC - Flag Control

001	Assert flag0	(t2)
000	Clear flag0	(t2)
011	Assert flag1	(t2)
010	Clear flag1	(t2)
1xx	Nil	

CCM - Channel Control Mux

When CCM equals zero, the control logic in the current channel associated with TBS. PSC, and PAC is configured according to the lower nine bits of the P register in the execution unit. Refer to Table 2-1 TPU Register Summary for a description of the bit fields of P when used for this purpose.

0	Use P register bits 0-8
1	Nil

MTD - Match/Transition Detect Service Request Inhibit Control

00	Enable service request
01	Inhibit service request
1x	Nil

B.4 Format 4: BRANCH, Flag, and RAM

B.4.1 Microengine/Sequencing Operations

RW - See B.4.3 RAM Operations

NMA - Next µPC Address Mode Control

00	Regular jump	(BAF → µPC)
01	Jump to subroutine	(BAF → µPC, if FLS = 1 then µPC + 1 → RAR else µPC → RAR)
10	Return from subroutine	(RAR → µPC)
11	Nil	

µPC Flush Control (FLS)

0	Flush instruction pipe (force microinstruction decode to NOP)
1	Nil

BAF - Branch Address Field

(9 bits)	
xxxxxxxxx	$000-$1FF

B.4.2 Channel Flag Control Operations

FLC - Flag Control

001	Assert flag0	(t2)
000	Clear flag0	(t2)
011	Assert flag1	(t2)
010	Clear flag1	(t2)
1xx	Nil	

LSR - Link Service Request Negation Control

0	Negate ISR
1	Nil

B.4.3 RAM Operations

RW - RAM Read/Write Control

0	Parameter access is a read (from RAM)
1	Parameter access is a write (to RAM)

IOM - RAM Input/Output Mode Control

000	P access using three-bit parameter number from AID (2:0) concatenated with channel number from channel register
001	P access using seven-bit address from DIOB (7:1)
010	P access using seven-bit address from AID (6:0)
100	DIOB access using three-bit parameter number from AID (2:0) concatenated with channel number from channel register
101	DIOB access using seven-bit address from DIOB (7:1)
110	DIOB access using seven-bit address from AID (6:0)
x11	Nil

AID - RAM Address/IImmediate Data Field

(7 bits) xxxxxxx $00-$7F

B.4.4 Microengine/Sequencing Operations

DEC/END - Decrementor/End State Control

00	Start decrement When DEC becomes one, the µPC is loaded from the return address register.
01	Start decrement µPC is not incremented while the decrementor is decrementing, until DEC becomes one.
10	End current state
11	Nil

B.5 Format 5: Execution Unit, Immediate, and FLAG

B.5.1 Execution Unit Operations

T1ABS - T1 A-Bus Source Control

BYTE Source

0000	AB(7:0)	= P(7:0);	AB(8:15)	=0	(t1)
0001	AB(7:0)	= P(15:8);	AB(8:15)	=0	(t1)
0010	AB(3:0)	= DEC(3:0);	AB(4:15)	=0	(t1)
0011	AB(7:4)	= CHAN(3:0);	AB(0:3), AB(8:15)	=0	(t1)
0111	AB(7:0)	= 00;	AB(8:15)	=0	(t1)

SPECIAL OPERATION (byte operation with respect to AU flags)

0100	AB(15:0)	=0;	ERT	=MER	(t2)

WORD Source

1000	AB(15:0)	= P(15:0)	(t1)
1001	AB(15:0)	= A(15:0)	(t1)
1010	AB(15:0)	= SR(15:0)	(t1)
1011	AB(15:0)	= DIOB(15:0)	(t1)
1100	AB(15:0)	= TCR1 (15:0)	(t1)
1101	AB(15:0)	= TCR2(15:0)	(t1)
1110	AB(15:0)	= ERT(15:0)	(t1)
1111	AB(15:0)	= 0000	(t1)

T3ABD - T3 A-Bus Destination Control

0000	A(15:0)	= AB(15:0)	(t3)
0001	SR(15:0)	= AB(15:0)	(t3)
0010	ERT(15:0)	= AB(15:0)	(t3)
0011	DIOB(15:0)	= AB(15:0)	(t3)
0100	P(15:8)	= AB(7:0)	(t3)
0110	P(7:0)	= AB(7:0)	(t3)
0111	P(15:0)	= AB(15:0)	(t3)
1000	LINK(3:0)	= AB(7:4)	(t3)
1001	CHAN(3:0)	= AB(7:4)	(t3)
1010	DEC(3:0)	= AB(3:0)	(t3)
1011	DEC(3:0)	= AB(3:0); CHAN(3:0) = AB(7:4)	(t3)
1100	TCR1 (15:0)	= AB(15:0)	(t3)
1101	TCR2(15:0)	= AB(15:0)	(t3)
1111	Nil (No destination is selected)		

SHF - AU Shifter Control

00 (Shift left)
AB(15:1) = AU(14:0), AB(0)- 0 (t3)
Carry latch = AU(15)

, ...

01 (Shift right)
if SRC=1 then
AB(14:0) = AU(15:1), AB(15) = Cout of AU (t3)
else
AB(14:0) = AU(15:1), AB(15) = 0 (t3)
Carry latch = AU(0)

10 (Rotate right)
AB(14:0) = AU(15:1), AB(15) = AU(0) (t3)
Carry latch = AU(0)

11 (No shift)
AB(15:0) = AU(15:0) (t3)
Carry latch = Cout of AU

NOTE

1. Cout represents the carryout of the AU-AU(16).
2. Carry latch represents the latch that is an input into the branch PLA
3. Encoding CCL controls the latching of the carry latch.
4. When SHF = 11 and a byte operation is performed, Cout is generated from the lower byte of the result. Otherwise, Cout is generated from the word result.

SRC - Shift Register Control

0 Shift right: SR(14:0) = SR(15:1)
If SHF = 01 then SR(15) = AU(0)
else SR(15) = 0;
1 No shift

CCL - AU Condition Latch Control

0 Latch conditions Z, C, N, and V into branch PLA (t3)
1 Do not latch conditions Z, C, N, and V

T1 BBI - T1 B-Bus Immediate Data

(8 bits)
xxxxxxxx 8 bits data field $00 - $FF (t1)

B.5.2 Channel Control Operations

LSR - Link Service Request Negation Control

0 Negate LSR
1 Nil

FLC - Flag Control

001	Assert flag0	(t2)
000	Clear flag0	(t2)
011	Assert flag1	(t2)
010	Clear flag 1	(t2)
1xx	Nil	

CIR - Channel Interrupt Request

0	Assert interrupt request	(t1)
1	Nil	

B.5.3 Microengine/Sequencing Operations

DEC/END - Decrementor/End State Control

00 Start decrement
When DEC becomes one, the µPC is loaded from the return address register.
01 Start decrement
µPC is not incremented while the decrementor is decrementing, until DEC becomes one.
10 End current state
11 Nil